

REMARKS

According to the response to the **previous** Office action dated 11/27/2007, applicant amended independent claims 1 and 12 to further include new claimed features in independent claims 1 and 12, in order to overcome the 35 U.S.C. 102 rejections of
5 claims 1 and 12 in the **previous** Office action dated 11/27/2007. In the following Office action dated 05/23/2008, Examiner considered the new claimed features added to independent claims 1 and 12, and then further cited another reference (Wulf et al.; US Patent No. 6,154,826) to make 35 U.S.C. 103 rejections of claims 1 and 12, respectively. Applicant appreciates and acknowledges Examiner's withdrawal of the 35 U.S.C. 102
10 rejections. However, applicant disagrees with Examiner's point of view regarding the independent claims 1 and 12 rejected under 35 U.S.C. 103.

35 U.S.C. 103 rejection

15 Claims 1-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delvaux et al. (US Patent No. 6,971,057) in view of Wulf et al. (US Patent No. 6,154,826).

Response

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Claim 1

For Examiner's convenience, previously presented claim 1 is listed below:

- 25 1. (previously presented) An apparatus for forming a sequence of N-byte second words from bytes forming a sequence of N-byte first words, where N is any integer greater than 1, the apparatus comprising:
a main memory for storing a plurality of bytes, each at a separate address;
a cache memory for storing a plurality of bytes, each at a separate address,

wherein and the size of the main memory is larger than that of the cache memory; and

5 a control circuit, **coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal**, for writing bytes of each first word into either the main memory or the cache memory **according to the control signal**, for reading bytes out of the cache memory or the main memory and forming each second word there from **according to the control signal**
10 such that each second word comprises bytes of more than one of the first words.

(emphases added)

Examiner points out that new reference Wulf et al. in combination with Delvaux
15 et al. teaches **comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal** (column 3, lines 39-62), (column 6, line 50 - column 7, line 11), (column 7, lines 47-58), (column 8, lines 24-30), (column 9, lines 19-27), (column 9, lines 42-52), (column 10, lines 16-41), (column 14, line 66 - column 15, line 9), (column 20, lines
20 13-32) and (column 22, lines 42-28). *(emphases added)*

Although the number of pages of Wulf's specification is almost ninety, most of the pages of Wulf's specification (e.g. almost 75% of the pages) are drawing figures for illustrating and comparing curves, where the curves are utilized for explaining Wulf's invention with different conditions/parameters applied.

25 Upon careful review, applicant respectfully points out that Wulf fails to disclose the claimed features **"comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a**

control signal” as recited in applicant’s claim 1. More particularly, none of Wulf’s paragraphs cited by Examiner teaches or suggests the above-identified claimed features.

For example, the paragraph under the heading "SUMMARY OF THE INVENTION" in Wulf’s disclosure (column 3, lines 39-62) only states some operations of the invention of Wulf without disclosing the claimed features such as “**comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal**”. (*emphases added*) In fact, Wulf is discussing something related to combining compile-time detection of memory access patterns with a memory subsystem (see column 6, lines 38-42 of Wulf’s disclosure).

In another example, the second, the third, the fourth and the fifth paragraphs under the heading "DETAILED DESCRIPTION OF THE INVENTION" in Wulf’s disclosure (column 6, line 50 - column 7, line 11) only state a solution of using "concurrency", and then say some disadvantages of using concurrent memory systems in certain conditions (e.g. with scalable computing system), where a calculation of a dot product is described merely for better comprehension regarding Wulf’s opinions. Again, the second, the third, the fourth and the fifth paragraphs under the heading "DETAILED DESCRIPTION OF THE INVENTION" fail to disclose the above-identified claimed features recited in applicant’s claim 1.

Please note that Wulf’s dot product of these paragraphs is utilized for explaining disadvantages of using concurrent memory systems in the certain conditions mentioned above, where Wulf’s dot product mentioned above is obtained by:

do 10, i=1, n

10 s=s+a(i)*b(i)

None of “(a(1), a(2), ..., a(n))” and “(b(1), b(2), ..., b(n))” discloses the “**data length, N**” recited in above-identified claimed features in applicant’s claim 1. (*emphases added*) In addition, none of “(a(1), a(2), ..., a(n))” and “(b(1), b(2), ..., b(n))” discloses the “**desired interleaving/de-interleaving depth, D**” recited in above-identified claimed

features in applicant's claim 1. (*emphases added*) Therefore, the dot product taught by Wulf is different from the product defined in above-identified claimed features "comparing the size of the cache memory with a **product of the data length, N and an desired interleaving/de-interleaving depth, D** to produce a control signal". (*emphases added*) Thus, Examiner makes the 35 U.S.C. 103 rejection of claim 1 based on misinterpretation of teachings of Wulf. Regarding this, Examiner might have occasionally described with **the benefit of hindsight** in order to **combine** the teachings of Wulf and Delvaux since Examiner's interpretation is neither taught nor suggested by Wulf and Delvaux.

The other paragraphs cited by Examiner (e.g., (column 7, lines 47-58), (column 8, lines 24-30), ..., and (column 22, lines 42-28)) are also carefully reviewed. However, they do not disclose the claimed features of applicant's claim 1, and more particularly, do not disclose the above-identified claimed features "**comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal**". (*emphases added*) For brevity, these remaining paragraphs cited by Examiner are not respectively explained in detail here.

As none of Wulf's paragraphs cited by Examiner teaches or suggests the claimed features such as "**comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal**", and as these paragraphs in combination still fail to disclose the above-identified claimed features, making rejections based on these paragraphs is improper or illogical. (*emphases added*)

Furthermore, in Examiner's opinion regarding patentability of claim 1, the applicant finds no meaningful connection or explanation of **why** Wulf's paragraphs cited by Examiner **really** teach or suggest the above-identified claimed features in applicant's claim 1.

In light of the above remarks, claim 1 is patentable over the combined teaching of the cited references. Withdrawal of the 35 U.S.C. 103 rejection is respectfully requested.

Claims 2-11 and 23-24

5 Claims 2-11 and 23-24 are dependent on claim 1, and should be allowed if claim 1 is found allowable.

Claim 12

10 In light of the above remarks under Claim 1, none of Wulf's paragraphs cited by Examiner teaches or suggests the claimed features such as **“comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal”** as recited in claim 12, and these paragraphs in combination still fail to disclose the above-identified claimed features in applicant's claim 12. (*emphases added*) Thus, claim 12 is patentable over the
15 combined teaching of the cited references. Withdrawal of the 35 U.S.C. 103 rejection of claim 12 is respectfully requested.

Claims 13-21 and 25-26

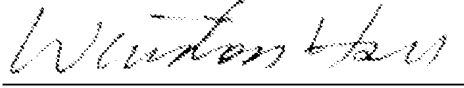
20 Claims 13-21 and 25-26 are dependent on claim 12, and should be allowed if claim 12 is found allowable.

Conclusion:

25 Thus, all pending claims are submitted to be in condition for allowance with respect to the cited arts for at least the reasons presented above. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)